

New patent claims

1. A semiconductor arrangement having at least one nonvolatile memory cell which has a first electrode which comprises at least two layers and has an organic material, the organic material forming a compound with that layer of the first electrode which is in direct contact, it being possible for the semiconductor arrangement to be produced by the following steps of:

5 10 - providing a first electrode, which comprises at least two layers and a layer of the first electrode may form a compound with an organic material;

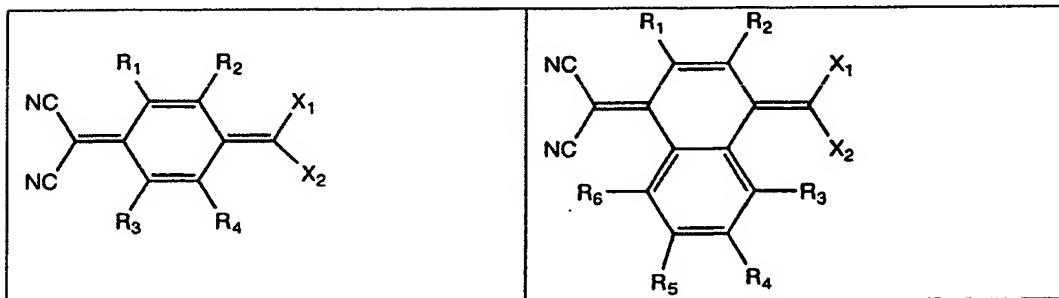
- contacting the first electrode with an organic material in order to form a compound; and

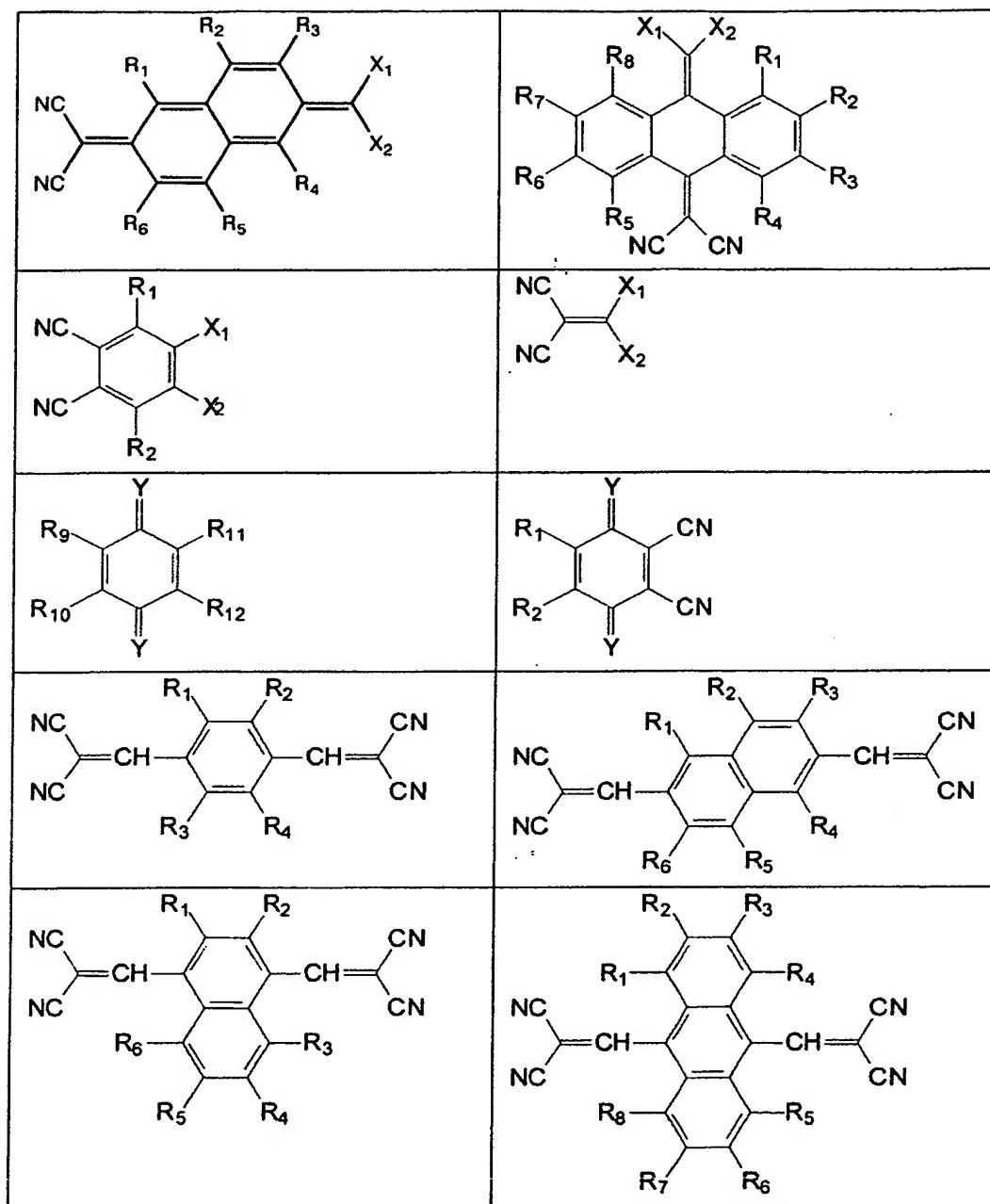
15 - forming a second electrode on the compound formed.

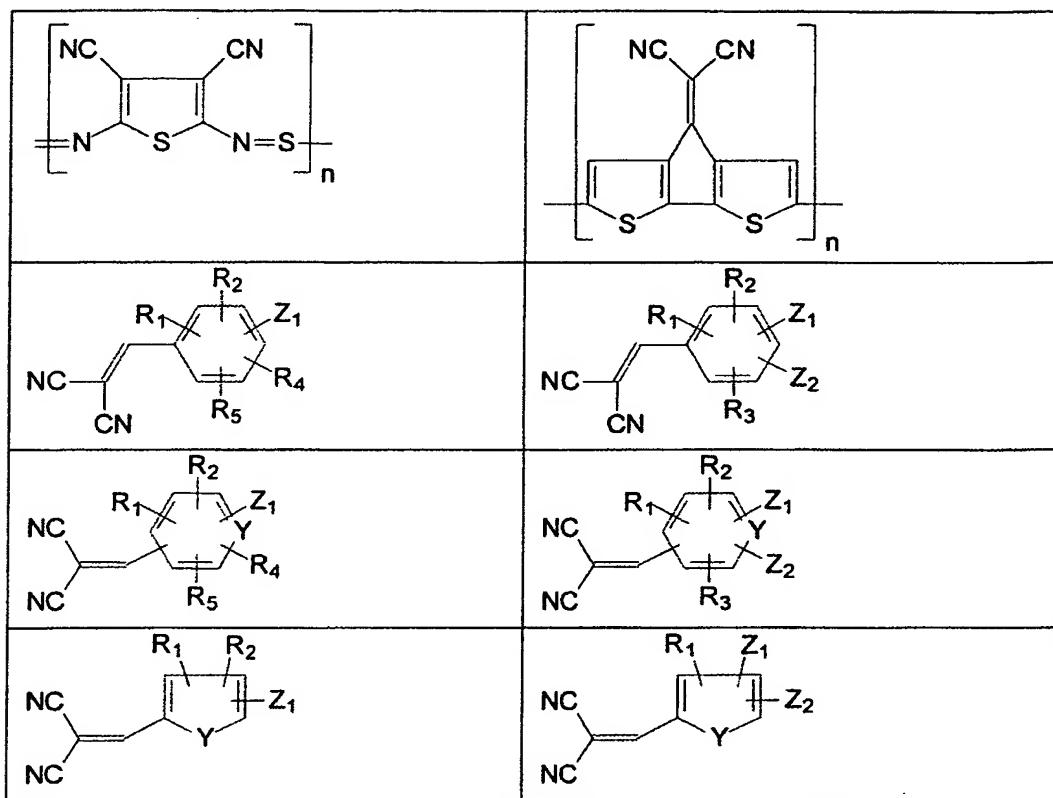
2. The semiconductor arrangement having a nonvolatile memory cell as claimed in claim 1,
wherein

20 the organic material has at least one of the following materials or compounds: sulphur, selenium or tellurium either in pure or in bonded form in particular as organocompounds of sulphur, selenium or tellurium, and sulphur-, selenium- or tellurium-containing oligomers or polymers, and/or one of the following compounds:

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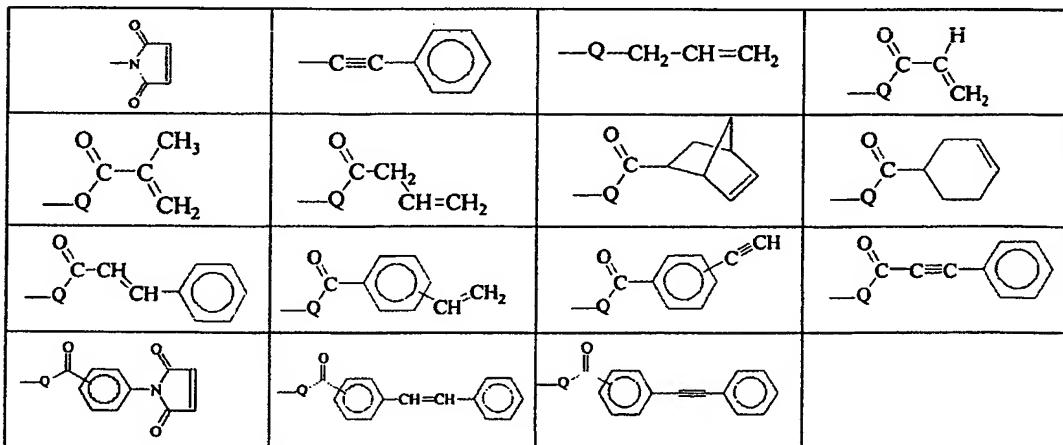




where R_1 , R_2 , R_3 , R_4 , R_5 , R_6 , R_7 and R_8 , independently of one another, have the following meaning:

5 H, F, Cl, Br, I (iodine), alkyl, alkenyl, alkynyl, O-alkyl, O-alkenyl, O-alkynyl, S-alkyl, S-alkenyl, S-alkynyl, OH, SH, aryl, heteroaryl, O-aryl, S-aryl, NH-aryl, O-heteroaryl, S-heteroaryl, CN, NO₂, -(CF₂)_n-CF₃, -CF((CF₂)_nCF₃)₂, -Q-(CF₂)_n-CF₃, -CF(CF₃)₂, -C(CF₃)₃ and

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n: n = 0 to 10

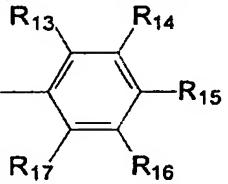
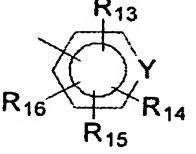
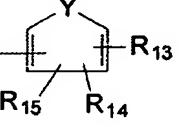
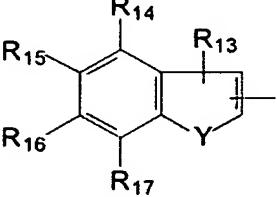
Q: -O-, -S-

5 R₉, R₁₀, R₁₁, R₁₂ may, independently of one another, be:
F, Cl, Br, I, CN, NO₂

R₁₃, R₁₄, R₁₅, R₁₆, R₁₇ may, independently of one another,
be:

10 H, F, Cl, Br, I, CN, NO₂

X₁ and X₂ may, independently of one another, be:

CN	
	
	

15

Y is: O, S, Se

and Z₁ and Z₂, independently of one another, are: CN,
NO₂.

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3. The semiconductor arrangement having a nonvolatile
memory cell as claimed in claim 1 or 2,
wherein

the organic material is an electron acceptor.

25

4. The semiconductor arrangement having a nonvolatile
memory cell as claimed in claim 3,

wherein

the electron acceptor has electron-attracting atoms or groups which are selected from: -Cl, -F, -Br, -I, -CN, -CO-, -NO₂.

5

5. The semiconductor arrangement having a nonvolatile memory cell as claimed in one of claims 1 to 4,
wherein

10 the organic material forms a charge transfer complex with the first electrode.

6. The semiconductor arrangement having a nonvolatile memory cell as claimed in one of claims 1 to 5,
wherein

15 that layer of the first electrode which is in contact with the organic material contains copper or silver.

7. The semiconductor arrangement having a nonvolatile memory cell as claimed in one of the preceding claims,

20 wherein

the organic material is present in a film thickness of between 30 and 1000 nm, preferably between 30 and 300 nm.

25 8. The semiconductor arrangement having a nonvolatile memory cell as claimed in one of the preceding claims,
wherein

the cell is scalable up to an area of 40 nm².

30 9. The semiconductor arrangement having a nonvolatile memory cell as claimed in one of the preceding claims,
wherein

that layer of the first electrode which is not in contact with the organic material is titanium (Ti),

35 titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), tungsten (W), TiW, TaW, WN, WCN, IrO, RuO, SrRuO, or a combination of said layers and/or materials

and, if appropriate, is additionally provided with a layer made of Si, TiNSi, SiON, SiO, SiC or SiCN.

10. The semiconductor arrangement having a nonvolatile
5 memory cell as claimed in one of the preceding claims,
wherein

the second electrode is made of aluminum, copper, AlCu,
AlSiCu, silver (Ag), titanium (Ti), titanium nitride
(TiN), tantalum (Ta), tantalum nitride (TaN), tungsten
10 (W), TiW, TaW, WN, WCN, IrO, RuO, SrRuO, or a
combination of said layers and/or materials and, if
appropriate, is additionally provided with a layer made
of Si, TiNSi, SiON, SiO, SiC or SiCN.

15 11. The semiconductor arrangement having a nonvolatile
memory cell as claimed in one of the preceding claims,
wherein

the cell can be switched between an ON state and an OFF
state.

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12. The semiconductor arrangement having a nonvolatile
memory cell as claimed in one of the preceding claims,
wherein

the ON and OFF states have different electrical
25 resistances.

13. The semiconductor arrangement having a nonvolatile
memory cell as claimed in claim 12,
wherein

30 the ratio between the ON and OFF states is more than
66.

14. A method for producing a nonvolatile memory cell
as claimed in one of the preceding claims,
35 characterized by the following steps of:

- providing a first electrode, which comprises at
least two layers and a layer of the first electrode may
form a compound with an organic material;

- contacting the electrode with an organic material in order to form a compound;
- and forming a second electrode on the compound formed.

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15. The method for producing a nonvolatile memory cell as claimed in claim 14,

wherein

10 the organic material is vapor-deposited onto the electrode under reduced pressure.

16. The method for producing a nonvolatile memory cell as claimed in claim 14,

wherein

15 the organic material is dissolved in a solvent in the process of contacting the first electrode.

17. The method as claimed in one of the preceding claims 14 to 16,

20 wherein

the organic material is subjected to a thermal treatment prior to forming the second electrode.

18. The method as claimed in one of claims 14 to 17,

25 wherein

prior to forming the second electrode, the excess organic material is rinsed with a solvent.

19. The method as claimed in claim 15,

30 wherein

the organic material is vapor-deposited at a pressure of between 0.00001 and 200 mbar.

20. The method as claimed in one of claims 14-19,

35 wherein

the contacting of the organic material takes place at a substrate temperature of between -50°C and 150°C.

21. The method as claimed in one of claims 14, 15, 17 to 20,

wherein

the organic material is mixed in the gas phase with a
5 carrier gas.

22. The method as claimed in one of claims 14 to 21,
wherein

10 prior to providing the second electrode, the compound formed is treated with an aftertreatment reagent.

23. The method as claimed in claim 22,
wherein

15 the aftertreatment reagent is selected from the following group: amines, amides, ethers, ketones, carboxylic acids, thioethers, esters, aromatics, heteroaromatics, alcohols or sulphur- or selenium-containing compounds.

20 24. The method as claimed in claim 23,
wherein

the sulphur-containing compounds are selected from the group containing: sulphur heterocyclic compounds, -SO-containing compounds and thiols.

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25. The method as claimed in one of claims 22-24,
wherein

the aftertreatment reagent is selected from the group containing:
diethylamine, triethylamine,
30 dimethylaniline, cyclohexylamine, diphenylamine,
dimethylformamide, dimethylacetamide, dimethyl sulfoxide, acetone, diethylketone, diphenylketone, phenyl benzoate, benzofuran, N-methylpyrrolidone, gamma-butyrolactone, toluene, xylene, mesitylene,
35 naphthalene, anthracene, imidazole, oxazole, benzimidazole, benzoxazole, quinoline, quinoxaline, fulvalene, furan, pyrrole, thiophene or diphenyl sulfide.

26. The method as claimed in one of claims 22 to 25,
wherein
the aftertreatment reagent is present in a solution.

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27. The method as claimed in one of claims 22-25,
wherein
the aftertreatment reagent is present as vapor.

10 28. The method as claimed in one of claims 22-27,
wherein
the aftertreatment time is between 15 seconds and 15
minutes.

15 29. The method as claimed in one of claims 22 to 28,
wherein
the aftertreatment takes place at a temperature of
-30°C to 150°C.

20 30. The method as claimed in one of claims 14-21,
wherein,
in the process of contacting the first electrode with
the organic material, the aftertreatment reagent as
claimed in one of claims 22-25 is admixed with the
25 solution containing the organic material or with the
vapor containing the organic material.

31. The semiconductor arrangement as claimed in one of
claims 1-13,
30 having the aftertreatment reagent as claimed in one of
claims 22-25, and/or a reaction product of the
aftertreatment reagent with the organic material and/or
the electrode material.

35 32. The semiconductor arrangement having a bit line
and a word line having a nonvolatile memory cell as
claimed in one of claims 1-13 and/or 31, the

nonvolatile memory cells being situated directly between bit and word lines that cross one another.

33. The semiconductor arrangement as claimed in
5 claim 32,

wherein

the nonvolatile memory cells are present in a plurality of layers.

10 34. The semiconductor arrangement as claimed in
claim 32 or 33,

which can be produced by the following steps in any desired order:

- forming at least one first interconnect on a
15 substrate, which serves as first electrode for the memory cell as claimed in one of claims 1-13 or 31;

- depositing an insulating layer;

- patterning the insulating layer, so that in the insulating layer trenches are patterned for at least
20 one interconnect transversely with respect to the first interconnects applied;

- depositing an organic material as claimed in one of claims 2 to 5;

- depositing at least one second electrode, which is
25 arranged transversely with respect to the first interconnect applied and serves as a second electrode for the memory cell.

35. The semiconductor arrangement as claimed in
30 claim 34,

wherein

the deposition of the insulating layer is effected after the deposition of the organic material.

35 36. The semiconductor arrangement as claimed in
claim 33,

which can be produced by the following steps in this order:

- forming at least one first interconnect on a substrate;
- depositing an insulating layer;
- patterning the contact holes above the first electrode;
- 5 depositing an organic material as claimed in one of claims 2-5 into the contact holes over the first electrode;
- depositing a second insulating layer;
- 10 patterning the second insulating layer, so that in the insulating layer trenches are patterned for at least one second interconnect, which runs transversely with respect to the first interconnects applied and covers the contact holes in the cell array;
- 15 depositing at least one second interconnect, which serves as a second electrode for the memory cell as claimed in one of claims 1-13 and/or 31.

37. The semiconductor arrangement as claimed in one of
20 claims 32 to 34,
wherein
it is produced by a Cu damascene technique.

38. A method for producing a semiconductor arrangement
25 as claimed in one of claims 32-37,
characterized by

- forming at least one first interconnect on a substrate, which serves as first electrode for the memory cell as claimed in one of claims 1-13 and/or 31;
- 30 depositing an insulating layer;
- patterning the insulating layer, so that in the insulating layer trenches are patterned for at least one interconnect transversely with respect to the first interconnects applied;
- 35 depositing an organic material as claimed in one of claims 2-5;
- depositing at least one second electrode, which is arranged transversely with respect to the first

interconnect applied and serves as a second electrode for the memory cell as claimed in one of claims 1-13 and/or 31.

5 39. The method as claimed in claim 38,
wherein

the deposition of the insulating layer is effected after the deposition of the organic material.

10 40. A method for producing a semiconductor arrangement as claimed in one of claims 32-37,

characterized by

- applying at least one first interconnect on a substrate;

15 - depositing an insulating layer;

- patterning the contact holes above the first electrode;

- depositing an organic material as claimed in one of claims 2-5 into the contact holes over the first

20 electrode;

- depositing a second insulating layer;

- patterning the second insulating layer, so that in the insulating layer trenches are patterned for at least one second interconnect, which runs transversely

25 with respect to the first interconnects applied and covers the contact holes in the cell array;

- depositing at least one second interconnect, which serves as a second electrode for the memory cell as claimed in one of claims 1-13 and/or 31.

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41. The method as claimed in one of claims 38-40,
wherein

after the deposition of the organic material, a protective layer is deposited on the organic material

35 prior to further processing.

42. A memory device containing a plurality of the nonvolatile memory cells as claimed in one of claims 1-13 and/or 31.

5 43. The memory device as claimed in claim 39,
wherein
a plurality of memory cells are arranged in one plane.

44. The memory device as claimed in claim 42 or 43,
10 wherein
a plurality of memory cells as claimed in one of claims 1 to 13 and/or 31 are arranged in the XY plane and in the XZ or YZ plane.